REMARKS

Claims 1-5 and 7-20 are pending in the present application. Replacement claim 9 has been presented herewith.

Claim Rejections-35 U.S.C. 112

Claim 9 has been rejected under 35 U.S.C. 112, second paragraph, because the claim includes insufficient antecedent basis for "the first temperature" in line 9. Claim 9 has been amended to feature in combination "performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature", to improve antecedent. Applicants respectfully submit that claim 9 is in compliance with 35 U.S.C. 112, second paragraph, and respectfully urge the Examiner to withdraw this rejection.

Claim Rejections-35 U.S.C. 103

Claims 1-5, 7, 8, 11 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Al-Shareef et al. reference (U.S. Patent No. 6,162,744), in view of the Ping et al. reference (U.S. Patent No. 5,882,979). This rejection is respectfully traversed for the following reasons.

The present application is directed to a method of manufacturing a capacitor of a semiconductor device, wherein the storage and plate electrodes consist of a noble metal such as Pt, Ru or Ir; a noble metal oxide such as RuO_2 or IrO_2; a conductive metal oxide such as $SrRuO_3$, $CaSrRuO_3$ or $BaSrRuO_3$; an alloy including Pt; an alloy including Ru; or an alloy including Ir. These noble metals may be grouped together and

characterized as catalytic noble metals. Since a catalytic noble metal as mentioned above is used, an annealing treatment must be performed at least one time in an oxidizing atmosphere in order to effectively remove oxygen vacancies and carbon impurities in the dielectric layer of the capacitor.

The catalytic noble metal plays an important role in the removal of oxygen vacancies and carbon impurities in the dielectric layer of the capacitor, because the catalytic noble metals better promote the disjointing of oxygen when it is annealed at a second temperature within an oxygen atmosphere, as compared to other metals. Also, catalytic noble metals have no problem oxidizing through the annealing process to become metal oxides having conductive characteristics.

With regard to the method for manufacturing a capacitor of claim 1, the first and second post-annealings are performed in-situ as a continuous annealing treatment. For example, the first annealing treatment may be performed at a high temperature and a reductive inert atmosphere for the crystallization of the dielectric layer. The second annealing treatment may be performed at a low temperature and oxygen atmosphere for curing the cystallized dielectric layer. These first and second annealing treatments if performed separately would each be 4 hour treatments respectively, for example. On the other hand, by performing the first and second post-annealings in-situ as in claim 1, the processing time is reduced to a total of approximately 2-3 hours for example, and throughput is improved by this continuous annealing treatment.

Applicants note that the in-situ processing in the Ping et al. reference is a general method to control and clean the surface of an amorphous silicon film prior to a

heat treatment step. The object and method of the in-situ processing of the Ping et al. reference is therefore completely different than that of the annealing in the Al-Shareef et al. reference. The object and method, and also the effects of the in-situ processing in the Ping et al. reference and the Al-Shareef et al. annealing, are different than that in the present application. That is, the two step in-situ annealing in the present application effects crystallization quality and leakage current of the dielectric layer, provides for an increase of the dielectric constant by improvement of crystallization and an increase of capacity of the capacitor as a result thereof, and reduces processing time. The prior art as relied upon by the Examiner does not specifically address these aspects. Applicants therefore respectfully submit that the method for manufacturing a capacitor of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1-5, 7, 8, 11 and 14 is improper for at least these reasons.

Claims 9, 10, 12, 13 and 15-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Al-Shareef et al. reference, in view of the Azuma et al. reference (WO 96/02067). This rejection is respectfully traversed for the following reasons.

The method for manufacturing a capacitor of a semiconductor device of claim 9 includes in combination performing the first and second post-annealings after the forming of the plate electrode. The advantages of such a two step annealing process after formation of the plate electrode is as follows.

Nucleation sites for crystallization of dielectric layer are simultaneously formed

between the storage electrode and dielectric layer, and between the plate electrode and the dielectric layer, if the subject annealings are performed after forming of the plate electrode. Accordingly, the method of claim 9 has the advantage that the temperature of the subject annealings are low compared to annealings performed prior to formation of the plate electrode. This prevents electrical characteristics from deteriorating because of deformation of the storage electrode. For example, deterioration of electrical characteristics such as leakage current in the dielectric layer because of physical damage such as cracks in the dielectric layer, and the induction of lifting between the storage electrode and the interdielectric layer, and lifting between conductive material over the storage electrode, can be prevented.

As noted above, catalytic noble metals have no problem oxidizing through the annealing process to be changed into metal oxides having conductive characteristics. However, in the Al-Shareef et al. reference as relied upon by the Examiner, the subject annealings are described in column 5, lines 6-11 as being conducted prior to formation of any portion of the plate electrode, in order to minimize the risk of oxidation of the plate electrode from any out-diffusion of oxygen from the high K capacitor dielectric layer. It is also noted that the Wolf reference merely explains general annealing methods such as densification and reflow about interdielectric layers in the semiconductor industry. Table 4 of the Wolf reference as relied upon by the Examiner does not specifically touch on the idea of performing post-annealings after formation of a plate electrode of a capacitor. With regard to the Azuma et al. reference, Fig. 4 shows first anneal step P47 occurring prior to formation of the second electrode in

steps P48 and P49.

Accordingly, Applicants respectfully submit that the method for manufacturing a capacitor of a semiconductor device of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 9 is improper for at least these reasons. Applicants also respectfully submit that the method of manufacturing a capacitor of claim 15 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 15-20 is improper for at least somewhat similar reasons.

The method for manufacturing a capacitor of claim 12 includes in combination first and second post-annealings being performed after forming of the interdielectric layer. The advantage of such a two step annealing after formation of the interdielectric layer are as follows.

An agglomeration layer can be formed if the plate electrode is very thin (50-300 angstroms) and the temperature of the post-annealings after the formation of the plate electrode is very high (over 650°C). In the method of claim 12 however, the interdielectric layer is formed over the plate electrode and the first and second post-annealings are performed thereafter. The interdielectric layer thus plays the role of a capping layer to prevent formation of an agglomeration layer. Also, the interdielectric layer can prevent the plate electrode from oxidizing in a follow up process, such as an annealing process in an oxidizing atmosphere. The prior art as relied upon by the Examiner does not specifically disclose first and second post-annealings being

performed after forming an interdielectric layer over a plate electrode, specifically for the purpose of preventing formation of an agglomeration layer. The prior art as relied upon by the Examiner does not disclose or suggest such above noted advantages of two step annealings after formation of an interdielectric layer. Accordingly, Applicants respectfully submit that the method of manufacturing a capacitor of a semiconductor device of claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

The following comments are offered responsive to the Examiner's remarks on page 10 of the Final Office Action dated January 30, 2002, to hopefully enable further understanding of the present application.

As to the remarks regarding oxidation of the barrier layer under the first storage electrode and the effects on capacitor leakage current and capacitance, it is noted that parasitic capacitances and resistances are formed if a barrier layer is oxidized. Such a device would effectively be an open circuit, and also the speed of the device is slowed. Oxidation of the barrier layer leads to deterioration of electrical characteristics and unexpected results. With regard to the post-anneals, it is noted that the first post-annealing is performed at a first temperature within an inert atmosphere for example, so that good characteristics of the high dielectric layer may be obtained. The second post annealing is performed at a second temperature in an oxidizing atmosphere for example, to remove oxygen vacancies which are formed after the first post-annealing Incidentally, the barrier layer is not oxidized because the first post-annealing is

performed within an inert atmosphere and the temperature of the second post-annealing is low enough to prevent oxidation of the barrier layer. Also, the use of catalytic noble metals increases curing effects for the removal of oxygen vacancies, because the catalytic noble metal promotes disjointing of oxygen as compared to other metals.

Conclusion

Claim 9 has been amended merely to improve form rather than to further distinguish over the relied upon prior art. Accordingly, the scope of claim 9 should not be considered as narrowed within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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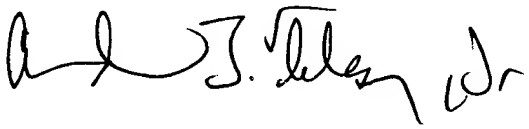

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Enclosures: Version with marked-up changes

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Claims:

9. (Twice Amended) A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode over the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature,

the first and second post-annealings being performed after the forming of the plate electrode.